PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference Opti95PCT	FOR FURTHER ACTION	See Form PCT/IPEA/416
International application No. PCT/NO2004/000361	International filing date *(day/month/year)* 24.11.2004	Priority date *(day/month/year)* 24.11.2003
International Patent Classification (IPC) or national classification and IPC INV. G11C8/06		
Applicant THIN FILM ELECTRONICS ASA et al.		

1. This report is the international preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.
2. This REPORT consists of a total of 5 sheets, including this cover sheet.
3. This report is also accompanied by ANNEXES, comprising:
   a. ☒ *sent to the applicant and to the International Bureau)* a total of 7 sheets, as follows:
      ☒ sheets of the description, claims and/or drawings which have been amended and are the basis of this report and/or sheets containing rectifications authorized by this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions).
      ☐ sheets which supersede earlier sheets, but which this Authority considers contain an amendment that goes beyond the disclosure in the international application as filed, as indicated in item 4 of Box No. I and the Supplemental Box.
   b. ☐ *(sent to the International Bureau only)* a total of (indicate type and number of electronic carrier(s)) , containing a sequence listing and/or tables related thereto, in electronic form only, as indicated in the Supplemental Box Relating to Sequence Listing (see Section 802 of the Administrative Instructions).

4. This report contains indications relating to the following items:

☒	Box No. I	Basis of the report
☐	Box No. II	Priority
☐	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
☐	Box No. IV	Lack of unity of invention
☒	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
☐	Box No. VI	Certain documents cited
☒	Box No. VII	Certain defects in the international application
☐	Box No. VIII	Certain observations on the international application

Date of submission of the demand	Date of completion of this report
22.06.2005	04.05.2006
Name and mailing address of the international preliminary examining authority: European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized officer Trifonov, A Telephone No. +49 89 2399-7168

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/NO2004/000361

Box No. I Basis of the report

1. With regard to the **language**, this report is based on

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into , which is the language of a translation furnished for the purposes of:
   - ☐ international search (under Rules 12.3(a) and 23.1(b))
   - ☐ publication of the international application (under Rule 12.4(a))
   - ☐ international preliminary examination (under Rules 55.2(a) and/or 55.3(a))

2. With regard to the **elements*** of the international application, this report is based on *(replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report)*:

   Description, Pages

   1-50 as published

   Claims, Numbers

   1-36 received on 19.04.2006 with letter of 19.04.2006

   Drawings, Sheets

   1-26 as published

   ☐ a sequence listing and/or any related table(s) - see Supplemental Box Relating to Sequence Listing

3. ☐ The amendments have resulted in the cancellation of:
   - ☐ the description, pages
   - ☐ the claims, Nos.
   - ☐ the drawings, sheets/figs
   - ☐ the sequence listing *(specify)*:
   - ☐ any table(s) related to sequence listing *(specify)*:

4. ☐ This report has been established as if (some of) the amendments annexed to this report and listed below had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).
   - ☐ the description, pages
   - ☐ the claims, Nos.
   - ☐ the drawings, sheets/figs
   - ☐ the sequence listing *(specify)*:
   - ☐ any table(s) related to sequence listing *(specify)*:

* *If item 4 applies, some or all of these sheets may be marked "superseded."*

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/NO2004/000361

Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	
	No:	Claims	1-36
Inventive step (IS)	Yes:	Claims	
	No:	Claims	1-36
Industrial applicability (IA)	Yes:	Claims	1-36
	No:	Claims	

2. Citations and explanations (Rule 70.7):

see separate sheet

Box No. VII Certain defects in the international application

The following defects in the form or contents of the international application have been noted:

see separate sheet

Re Item V.

1 Reference is made to the following documents:

D1: WO 02 05287 A1
D2: WO 03 046923 A1

2 The present application does not meet the criteria of Article 33(1) PCT, because the subject-matter of claim 1 is not new in the sense of Article 33(2) PCT.

Document D1 discloses a method of driving a data storage apparatus comprising a passive matrix comprising further bit lines, word lines and memory cells of electrically polarizable material exhibiting hysteresis. The method (see Abstract and Fig. 4) comprises a first addressing operation directed to a first memory segment including the following steps executed in accordance with a predetermined pulse protocol:
- setting an addressed data storage cell to a first polarization state by applying a first voltage pulse, as disclosed in D1 - reset step (t1-t2) in Fig. 4;
- applying a second voltage pulse of opposite polarity to that of the first voltage pulse and switching the polarization state of the addressed data storage cell from the first to a second polarization state, as disclosed in D1 - set step (t5-t6) in Fig. 4.

It is further known to the skilled man that the memory devices consist not of a single matrix but are hierarchically structured comprising electrically separated sub matrices and segments. Accordingly, the features of the characterising portion of claim 1:
- applying a second addressing operation to one or more cells in another memory segment, different than the first memory segment where the first addressing operation is executed, and;
- dependent on the addressing operation to be carried out, storing information in said cell or cells,
are considered as a logical repetition of the first addressing operation this time in a different memory segment.

Independent claim 1 lacks, therefore, novelty compared with the prior art of D1.

3 The rest of the claims, dependent of claim 1, concern features like management of address mapping tables (logical-to-physical address translation tables) and add nothing new or inventive to claim 1.

4 The present application as a whole comprises subject-matter which is considered, when appropriately defined, to conform the requirements of the PCT for novelty and inventive step.

It is stated in the description (see pg, 15, ln. 20-21) a method of reduction the consecutive addressing in the same segment by directing data addressed by an operation to another segment. A memory device, as described in the preamble of claim 1, its corresponding memory operation complying to said method and characterized by:
- setting an addressed first data storage cell to a first polarisation state by means of a first active voltage pulse in a first operation;
- applying a second active voltage pulse of opposite polarity to that of the first active voltage pulse to a second storage cell, different than that subjected to the first active voltage pulse in a second operation;
- said first and second storage cells are located in **different** memory segments;
- said first and second operations are **consecutive** operations;
- redirection of addressed data from the first to the second segment,
would seems to satisfy the requirements of PCT.

Re Item VII.

- reference signs are not inserted in parentheses in the claims in accordance with Rule 6.2(b) PCT.

CLAIMS

1. A method for reducing detrimental phenomena related to disturb voltages in a data storage apparatus employing passive matrix-addressing, particularly a memory device or a sensor device, wherein the data storage apparatus comprises a plurality of data storage cells for storing logical values as given by a specific charge value set in each cell, wherein each of the data storage cells comprises an electrically polarizable memory material exhibiting hysteresis, particularly a ferroelectric or electret material, wherein the cells are physically disposed in one or more matrices, wherein each of said matrices providing passive matrix addressability to the cells, wherein each of the matrices comprising a first and a second electrode set, wherein the electrodes of each set are provided in parallel, one set of electrodes forming word lines and the other set forming bit lines, wherein the word line electrodes and the bit line electrodes are provided crossing each other and in direct or indirect contact with the memory material, wherein the data storage cells of the apparatus are realized as capacitor-like elements defined in a volume of the memory material between or at the crossings of word lines and bit lines and can be set to either of at least two polarization states or switched therebetween by applying an active voltage pulse of a voltage V_S larger than the coercive voltage V_C corresponding to the coercive electric field of the memory material, between a word line and a bit line and over the data storage cell defined therebetween, wherein an application of electric potentials conforms to an addressing operation, and wherein the electric potentials applied to all word and bit lines in the addressing operation are controlled in a time-coordinated manner according to a predetermined voltage pulse protocol,
~~characterized by~~ wherein the data storage cells of the data storage apparatus are provided in two or more electrically separated segments, each segment comprising a separate physical address space of the data storage apparatus, wherein a first addressing operation comprises setting ~~an~~ one or more addressed data storage ~~cell~~ cells in one of the segments to a first polarization state by means of a first active voltage pulse in the addressing operation, during which each bit line dependent on the voltage pulse protocol can be connected with a sensing means for detecting the polarization state of the data storage cell at least under a part of the duration of the first active voltage pulse~~;~~ applying dependent on the voltage pulse protocol a second voltage pulse, which can be a second active voltage pulse of opposite polarity

to that of the first active voltage pulse and switching the addressed data storage cell from the first polarization state to a second polarization state, such that the cell being addressed is set to a predetermined polarization state as specified by the addressing operation, ~~providing the data storage cells of the data storage apparatus employing passive matrix addressing in two or more electrically separated segments, each segment comprising a separate physical address space of the data storage apparatus; and directing data in the addressing operation to a segment that is selected based on information on prior and/or scheduled applications of active voltage pulses in the segments.~~, characterized by further applying in the second addressing operation the second voltage pulse to one or more data storage cells in another segment, such that the cell or cells are preset to either the first polarization state or the second polarization state; and dependent on the addressing operation to be carried out, storing information in said one of more preset data storage cells in the other segment after an active voltage pulse with the same polarity has been applied thereto; said another segment being selected for the second addressing operation on the basis of prior and/or scheduled application of active voltage pulses to said two or more electrically separated segments.

~~2. A method according to claim 1, characterized by applying the second voltage pulse to another cell than that subjected to the first active pulse, whereby all cells at the physical address of the other cell are pre-set to either the first polarization state or to the second polarization state and are located in a segment different than that subjected to the first active voltage pulse.~~

~~3. A method according to claim 1, characterized by explicitly storing information on cells at a certain address and which are pre-set to a polarization state after an active voltage pulse of same polarity has been applied to each cell at the address.~~

42. A method according to claim ~~3~~1, characterized by storing information on the pre-set polarization state with reference to the physical address of the cell.

53. A method according to claim 31, characterized by retrieving the stored information on the polarization state prior to subjecting a cell to the second voltage pulse.

64. A method according to claim 53, characterized by applying the optional second active voltage pulse with opposite polarity to the first active voltage pulse if the pre-set polarization corresponds to the first polarization state, and applying the optional second active voltage pulse with same polarity as the first active voltage pulse if the pre-set polarization corresponds to the second polarization state.

75. A method according to claim 31, characterized by removing the stored information on the cell being pre-set to a polarization state after subjecting each of the pre-set cells at the address to the second voltage pulse.

86. A method according to claim 31, characterized by storing information on the total number of pre-set cells.

97. A method according to claim 1, characterized by directing data in an addressing operation to the segment with the longest time since last being subjected to an active voltage pulse.

108. A method according to claim 97, characterized by using a queue; putting a reference to the segment most recently subjected to an active voltage pulse last in the queue and retrieving a reference to the segment with the longest time since being subjected to an active pulse from first position in the queue.

119. A method according to claim 910, characterized by storing references to each of the segments in a "segment table" with additional information connected to each of the references.

1210. A method according to claim 119, characterized by the additional information being number of addresses with pre-set cells in the referenced segment and/or timestamp of last segment access and/or lock state mark and/or physical addresses to pre-set cells in the referenced segment and/or a pre-set polarization state mark connected to each of the physical addresses to pre-set cells.

~~13~~11. A method according to claim ~~12~~10, characterized by removing the physical address of the cell subjected to the second voltage pulse from the segment table.

~~14~~12. A method according to claim ~~12~~10, characterized by adding the physical address of the cell subjected to the first active voltage pulse to the segment table.

~~15~~13. A method according to claim ~~12~~10, characterized by setting the lock state mark of a segment reference in the segment table when the first active voltage pulse or the second voltage is applied to a cell in the segment corresponding to the segment reference.

~~16~~14. A method according to claim ~~12~~10, characterized by updating the timestamp of last segment access of a segment reference in the segment table when the first active voltage pulse or the second voltage pulse is applied to a cell in the segment corresponding to the segment reference.

~~17~~15. A method according to claim ~~12~~10, characterized by unsetting the lock state mark of a segment reference in the segment table when the difference between current time and the timestamp of last segment access for the segment reference exceeds a predetermined value.

16. A method according to claim 10, characterized by waiting to apply the first active voltage pulse until the lock state mark of the segment to be subjected to the first active voltage pulse has been unset, and/or waiting to apply the second voltage pulse until the lock state mark of the segment to be subjected to the second voltage pulse has been unset

~~18~~17. A method according to claim 1, characterized by storing the physical address of the cell subjected to the second voltage pulse with reference to the logical address of the addressing operation.

~~19~~18. A method according to claim ~~18~~17, characterized by storing the physical address with reference to the logical address in an "address mapping table" with optional address level

information connected to each of the physical address entries in the address mapping table.

~~20~~19. A method according to claim ~~19~~18, characterized by the address level information being a pre-set mark and/or a pre-set polarization state mark and/or a segment reference.

~~21~~20. A method according to claim ~~19~~18, characterized by storing the address mapping table in a fast access memory other than the data storage apparatus employing passive matrix-addressing.

~~22~~21. A method according to claim ~~19~~18, characterized by not listing a predetermined number of addresses to pre-set cells in the address mapping table.

~~23~~22. A method according to claim ~~19~~18, characterized by retrieving the physical address with the address level information from the address mapping table before applying the first active voltage pulse and/or the second voltage pulse.

~~24~~23. A method according to claim ~~23~~22, characterized by not applying the first active voltage pulse and bringing the second voltage pulse forward in time if finding a set pre-set mark.

~~25~~24. A method according to claim ~~23~~22, characterized by not applying the first active voltage pulse and bringing the second voltage pulse forward in time if the addressing operation is write and if the address of the pre-set cells is listed in the address mapping table.

~~26~~25. A method according to claim ~~23~~22, characterized by not applying the first active voltage pulse and bringing the second voltage pulse forward in time if the addressing operation is write and if the total number of pre-set cell addresses are exceeding a predetermined value.

~~27~~26. A method according to claim ~~18~~17, characterized by storing the logical address in part of the data storage cells at the physical address corresponding to the logical address.

~~28~~27. A method according to claim 1, characterized by distributing addresses whereat each cell are pre-set to the

same polarization state among the segments during idle time when no other higher-priority operations are ongoing or imminent in the segments.

~~29~~28. A method according to claim ~~28~~27,
characterized by executing a read with write-back operation in the segment with the least number of pre-set cells.

~~30~~29. A method according to claim 1,
characterized by creating cells that are pre-set to the same polarization state at a free address during idle time when no other higher-priority operations are ongoing or imminent in the segments.

~~31~~30. A method according to claim ~~30~~29,
characterized by applying a single polarity active voltage pulse to each cell at the address.

~~32~~31. A method according to claim ~~30~~29,
characterized by selecting the address in the segment with the least number of pre-set cells

~~33~~32. A method according to claim 1,
characterized by imposing a delay before applying the first active voltage pulse if the second voltage pulse of the preceding operation, or any of a predetermined number of preceding operations, was applied to the same segment as the current addressing operation.

~~34~~33. A method according to claim 1,
characterized by imposing a delay before applying the first active voltage pulse if the difference between current time and the last time the segment was subjected to a first active voltage pulse or a second voltage pulse does not exceed a predetermined value.

~~35~~34. A method according to claim 1,
characterized by imposing a delay before applying the second active voltage pulse if the difference between current time and the last time the segment was subjected to a first active voltage pulse or a second voltage pulse, does not exceed a predetermined value.

~~36. A method according to claim 12,~~
~~characterized by waiting to apply the first active voltage pulse until the lock state mark of the segment to be subjected to the first active voltage pulse has~~

~~been unset, and/or waiting to apply the second voltage pulse until the lock state mark of the segment to be subjected to the second voltage pulse has been unset.~~

~~37~~35. A method according to claim 1, characterized by analyzing the consecutive operation or a predetermined number of consecutive operations before executing the current addressing operation.

~~38~~36. A method according to claim ~~37~~35, characterized by selecting another segment than addressed by the consecutive operation or by a predetermined amount consecutive operations for application of the second voltage pulse of the current addressing operation.